HANCHEN YE

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EDUCATION

- **University of Illinois at Urbana-Champaign**, Urbana, IL
  Ph.D. in Electrical and Computer Engineering — *Aug. 2019 - Present*
  Thesis Advisor: Prof. Deming Chen
- **Fudan University**, Shanghai, China
  M.E. in Integrated Circuit Engineering — *Sep. 2017 - Jun. 2019*
- **Fudan University**, Shanghai, China
  B.E. in Microelectronic Science and Engineering — *Sep. 2013 - Jun. 2017*
- **National University of Singapore**, Singapore
  Exchange Student in Electrical and Computer Engineering — *Aug. 2015 - Dec. 2015*

WORK EXPERIENCES

- **University of Illinois at Urbana-Champaign**, Urbana, IL
  Research Assistant, Electrical and Computer Engineering Department — *Aug. 2019 - Present*
  Advisor: Prof. Deming Chen
- **Inspirit IOT**, Champaign, IL (Virtual)
  Part-time Intern — *Jan. 2024 - May 2024*
  Advisor: Prof. Deming Chen
- **Google**, Mountain View, CA
  Ph.D. Resident, X, The Moonshot Factory — *May 2023 - Aug. 2023*
  Advisor: Xiaoqing Xu, Prof. David Z. Pan, Chris Leary
- **Intel**, Portland, OR (Virtual)
  Research Intern, Strategic CAD Labs — *May 2022 - Aug. 2022*
  Advisor: Jin Yang, Jeremy Casas, Zhenkun Yang
- **SiFive**, San Mateo, CA (Virtual)
  Compilers Intern, Platform Engineering Department — *May 2021 - Aug. 2021*
  Advisor: Andrew Lenharth
- **Xilinx (AMD)**, San Jose, CA (Virtual)
  Compiler Intern, Research Labs — *Jun. 2020 - Aug. 2020*
  Advisor: Stephen Neuendorffer
- **Fudan University**, Shanghai, China
  Research Assistant, State Key Laboratory of ASIC and System — *Sep. 2016 - Jun. 2019*
  Advisor: Prof. Gengsheng Chen

AWARDS AND SCHOLARSHIPS

- SRC TECHCON **First Place Best Student Presenter Award** — *Sep. 2023*
- DAC Ph.D. Forum **First Place Winner** — *Jul. 2023*
- UIUC **A.R. Buck Knight Fellowship** — *Apr. 2023*
- AMD **HACC Outstanding Researcher Awards** — *Feb. 2023*

- UIUC **Teachers Ranked as Excellent** *Fall 2022*
- UIUC **Rambus Computer Engineering Fellowship** *May 2022*
- DAC **Young Fellows** *Jun. 2020, Apr. 2022*
- Shanghai **Outstanding Graduates** *Jun. 2019*
- Fudan University **KLA-Tencor Scholarship** *Dec. 2018*
- Fudan University **Outstanding Graduate Students** *Oct. 2018*
- The 2nd China College IC Competition **Grand Prize Winner** *Aug. 2018*
- Fudan University **Xi-Yuan Research Scholarship** *May 2016*
- Fudan University **Outstanding Undergraduate Students** *Dec. 2015*

PUBLICATIONS

[1] **ScaleHLS-HIDA: From PyTorch/C++ to Highly-optimized HLS Accelerators (Tutorial)**
Hanchen Ye and Deming Chen
The ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), 2024

[2] **Subgraph Extraction-based Feedback-guided Iterative Scheduling for HLS**
Hanchen Ye, David Z. Pan, Chris Leary, Deming Chen, and Xiaoqing Xu
The Conference on Design, Automation & Test in Europe (DATE), 2024

[3] **HIDA: A Hierarchical Dataflow Compiler for High-Level Synthesis**
Hanchen Ye, HyeGang Jun, and Deming Chen
The ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2024

[4] **Software/Hardware Co-design for LLM and Its Application for Design Verification (Invited)**
Jiaxin Wan*, Yingbing Huang*, Yuhong Li, **Hanchen Ye**, Jinghua Wang, Xiaofan Zhang, and Deming Chen (* equal contributors)
The Asia and South Pacific Design Automation Conference (ASP-DAC), 2024

[5] **ScaleFlow: High-Level Synthesis for Large Dataflow Applications**
Hanchen Ye and Deming Chen
The Semiconductor Research Corporation (SRC) TECHCON, 2023

[6] **High-Level Synthesis for Domain Specific Computing (Invited)**
Hanchen Ye, Hyegang Jun, Jin Yang, and Deming Chen
The ACM International Symposium on Physical Design (ISPD), 2023

[7] **CHARM: Composing Heterogeneous Accelerators for Matrix Multiply on Versal ACAP Architecture**
Jinming Zhuang, Jason Lau, **Hanchen Ye**, Zhuoping Yang, Yubo Du, Jack Lo, Kristof Denolf, Stephen Neuendorffer, Alex Jones, Jingtong Hu, Deming Chen, Jason Cong, and Peipei Zhou
The ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), 2023

[8] **AutoScaleDSE: A Scalable Design Space Exploration Engine for High-Level Synthesis**
HyeGang Jun, **Hanchen Ye**, Hyunmin Jeong, and Deming Chen
The ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2022

[9] **ScaleHLS: a Scalable High-Level Synthesis Framework with Multi-level Transformations and Optimizations (Invited)**
Hanchen Ye, HyeGang Jun, Hyunmin Jeong, Stephen Neuendorffer, and Deming Chen
The ACM/IEEE Design Automation Conference (DAC), 2022

[10] **ScaleHLS: A New Scalable High-Level Synthesis Framework on Multi-Level Intermediate Representation**
Hanchen Ye, Cong Hao, Jianyi Cheng, Hyunmin Jeong, Jack Huang, Stephen Neuendorffer, and Deming Chen
The IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2022

[11] **Being-ahead: Benchmarking and Exploring Accelerators for Hardware-Efficient AI Deployment**
Xiaofan Zhang, **Hanchen Ye**, and Deming Chen
The Workshop on Benchmarking Machine Learning Workloads on Emerging Hardware (MLBench) of the Conference on Machine Learning and Systems (MLSys), 2021

[12] **ScaleHLS: Achieving Scalable High-Level Synthesis through MLIR**
Hanchen Ye, Cong Hao, Hyunmin Jeong, Jack Huang, and Deming Chen
The Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE) of the ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2021

[13] **DNNExplorer: A Framework for Modeling and Exploring a Novel Paradigm of FPGA-based DNN Accelerator**
Xiaofan Zhang*, **Hanchen Ye***, Junsong Wang, Yonghua Lin, JinJun Xiong, Wen-mei Hwu, and Deming Chen (* equal contributors)
The ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2020

[14] **IDLA: An Instruction-based Adaptive CNN Accelerator**
Peng Gao, Zhize Huang, **Hanchen Ye**, and Gengsheng Chen
The IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2020

[15] **HybridDNN: A Framework for High-Performance Hybrid DNN Accelerator Design and Implementation**
Hanchen Ye, Xiaofan Zhang, Zhize Huang, Gengsheng Chen, and Deming Chen
The ACM/IEEE Design Automation Conference (DAC), 2020

[16] **A Resource-Sharing & Pipelined Design Scheme for Dynamic Deployment of CNNs on FPGAs**
Hanchen Ye and Gengsheng Chen
The IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2018

POSTERS

[1] **ScaleHLS: A Scalable High-Level Synthesis Framework**
Hanchen Ye and Deming Chen
Ph.D. Forum of the ACM/IEEE Design Automation Conference (DAC), 2023

[2] **vHLS: Verifiable and Efficient High-Level Synthesis**
Hanchen Ye and Deming Chen
Student Research Contest (SRC) of the ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2022

[3] **ScaleFlow: Scalable High-Level Synthesis for Large Dataflow Applications**
Hanchen Ye and Deming Chen
Accelerated AI Algorithms for Data-Driven Discovery (A3D3) Annual Meeting, 2022

[4] **PolyAIE: A Dataflow Compiler for Heterogeneous Compute Platforms**
Hanchen Ye and Deming Chen
Young Fellow Program of the ACM/IEEE Design Automation Conference (DAC), 2022

PATENTS

[1] **Special-shaped Pipeline Design Method Based on FPGA Local Dynamic Reconstruction Technology**
Gengsheng Chen, **Hanchen Ye**, Siyu Ni, and Chao Huang
China Patent CN108228966B, 2017

TALKS AND PRESENTATIONS

- **HIDA: A Hierarchical Dataflow Compiler for High-Level Synthesis**
  Intel HLD (High-level Design) Reading Group — *Feb. 2024*
  AMD-UIUC Center of Excellence Seminars — *Nov. 2023*
- **Scalable High-Level Synthesis for AI Accelerator Design and Verification**
  UIUC Ph.D. Preliminary Exam — *Oct. 2023*
- **MLIR, ScaleHLS, and HIDA**
  UIUC ECE527 (System-On-Chip Design) Guest Lecture — *Oct. 2023*
- **ScaleFlow: Scalable High-Level Synthesis for Dataflow Applications**
  Semiconductor Research Corporation (SRC) TECHCON — *Sep. 2023*
  Google X Journal Club — *Feb. 2023*
- **MLIR and ScaleHLS**
  UIUC ECE527 (System-On-Chip Design) Guest Lecture — *Oct. 2022*
- **Hardware Compilation with MLIR and CIRCT**
  Intel Strategic CAD Labs (SCL) Tech Presentation — *Jul. 2022*
- **ScaleHLS: A Scalable High-Level Synthesis Framework on MLIR**
  Symposium on High-Performance Computer Architecture (HPCA) — *Apr. 2022*
  FPGA Workshop on Open-Source Source-to-Source Transformation for HLS — *Feb. 2022*
  UIUC CS Compiler Seminar — *Nov. 2021*
  UIUC ECE527 (System-On-Chip Design) Guest Lecture — *Nov. 2021*
  Xilinx Adaptive Compute Clusters (XACC) Tech Talk Series — *Aug. 2021*
  UCSC Hardware Systems Collective (HSC) Seminar — *May 2021*
  ASPLOS Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE) — *Apr. 2021*
- **Compilers for Domain-Specific Accelerators**
  Gatech ECE6100/CS6290 (Advanced Computer Architecture) Guest Lecture — *Dec. 2021*
  CCF Agile Hardware Development and Open-Source EDA Forum — *Jun. 2021*
- **FSM (Finite-State Machine) Dialect in CIRCT**
  Circuit IR Compilers and Tools (CIRCT) Open Meeting — *Aug. 2021*
- **Handshake-based High-Level Synthesis in CIRCT**
  Open-Source Development Tools (OSDT) Open Meeting — *Aug. 2020*
  Circuit IR Compilers and Tools (CIRCT) Open Meeting — *Aug. 2020*
- **HybridDNN: A Framework for High-Performance Hybrid DNN Accelerator Design and Implementation**
  UIUC Ph.D. Qualifying Exam — *Oct. 2020*
  Design Automation Conference (DAC) — *Jul. 2020*
- **A Resource-Sharing and Pipelined Design Scheme for Dynamic Deployment of CNNs on FPGAs**
  Conference on Solid-State and Integrated Circuit Technology (ICSICT) — *Nov. 2018*

SELECTED PROJECTS

- **XLS: Accelerated HW Synthesis** *May. 2023 - Present*
  - XLS implements a High Level Synthesis (HLS) toolchain which produces synthesizable designs (Verilog and SystemVerilog) from flexible, high-level descriptions of functionality.
  - Proposed a feedback-directed optimization (FDO) method that takes downstream tools (e.g., OpenROAD) results as feedback to improve SDC scheduling quality.

- **HIDA: A Hierarchical Dataflow Compiler for High-Level Synthesis** *Mar. 2022 - Present*
  - Proposed two-level dataflow representations for modeling hierarchical dataflow structures in HLS.
  - Designed an automated optimizer that decomposes the dataflow optimization problem into multiple levels, achieving scalable task partitioning, dataflow scheduling, and parallelization.

- **PolyAIE: A Polyhedral Compiler for Xilinx ACAP** *Oct. 2021 - Present*
  - Map C/C++ programs or PyTorch models to the AI-Engine (AIE) array and Programming Logic (PL) on Xilinx ACAP using Polyhedral compilation techniques in MLIR.

- **CIRCT: Circuit IR Compilers and Tools** *Jun. 2020 - Present*
  - The CIRCT open-source project is an effort looking to apply MLIR and the LLVM development methodology to the domain of hardware design tools;
  - Contributed to the FIRRTL, HW (Hardware), and SV (SystemVerilog) dialects to establish the core IR of hardware and enable a Chisel to SystemVerilog compilation flow;
  - Contributed a new FSM dialect to represent, optimize, and generate codes for finite-state machines;
  - Contributed to the Handshake and Pipeline dialects to enable a High-Level Synthesis (HLS) flow, which is a compilation pipeline from high-level programs to gate-level circuits.

- **ScaleHLS: A Scalable High-Level Synthesis Framework on MLIR** *Apr. 2020 - Present*
  - Proposed and designed a hierarchical HLS representation and optimization methodology in MLIR;
  - Designed a transform and analysis library dedicated for HLS applications;
  - Designed an HLS C front-end and a synthesizable C/C++ emission back-end for MLIR.

- **DNNExplorer: A Novel Design Paradigm of DNN Accelerator** *Feb. 2020 - Mar. 2021*
  - Proposed a novel paradigm which can take advantage of both pipeline and generic architecture;
  - Proposed an efficient design space exploration algorithm to generate optimized DNN accelerators following the new paradigm.

- **HybridDNN: Hybrid Spatial and Winograd DNN Accelerator** *Jan. 2019 - Dec. 2019*
  - Proposed a hybrid Spatial and Winograd convolution architecture for DNN acceleration;
  - Designed a comprehensive tool for the performance and area estimation and the design space exploration for both edge and cloud FPGAs.

- **Musket: RISCV-based IoT Sensor-Hub on FPGA** *Apr. 2018 - Aug. 2018*
  - Pruned and transplanted a RISCV core to an edge FPGA and established a low-power SoC;
  - Ported an RTOS to manage sensors and the wireless connection between FPGA and smartphones;
  - Won the outstanding award of the 2nd China College IC Competition.

- **Dynamic and Pipelined CNN Accelerator on FPGA** *Oct. 2017 - May 2018*
  - Proposed a Dynamic Partial Reconfiguration (DPR) -based pipeline architecture to deploy large CNN accelerators on resource-limited FPGAs while maintaining a low overall latency.

PROFESSIONAL SERVICES

- **Program Committee**
  ASPLOS Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE) *2022, 2023*

- **Reviewer**
  Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) *2021 - 2023*
  Springer Neural Processing Letters (NEPL) *2021*

- **External Reviewer**
  International Conference on Computer-Aided Design (ICCAD) *2023*
  International Symposium on Field-Programmable Custom Computing Machines (FCCM) *2022 - 2024*
  International Symposium on Field-Programmable Gate Arrays (FPGA) *2021, 2023, 2024*

TEACHING SERVICES

- **Teaching Assistant**
  UIUC ECE527: System-On-Chip Design *Fall 2022, Fall 2023*
- **Guest Lecture**
  UIUC ECE527: System-On-Chip Design *Fall 2021, Fall 2022, Fall 2023*
  Gatech ECE6100/CS6290: Advanced Computer Architecture *Fall 2021*

SELECTED COURSES

- **CS 526:** Advanced Compiler Construction (A) *Spring 2021*
- **ECE 527:** System-On-Chip Design (A+) *Fall 2020*
- **ECE 549:** Computer Vision (A) *Spring 2020*
- **ECE 598 NSG:** Deep Learning in Hardware (A+) *Fall 2019*
- **ECE 598 MS:** Adv Memory & Storage Systems (A) *Fall 2019*

TECHNICAL SKILLS

Programming Languages	Verilog HDL, C++, Python, Cuda, Tcl, etc.
Frameworks & Tools	Vivado/Vitis, Vivado/Vitis HLS, PyTorch, LLVM, MLIR, LaTeX, etc.